IN THE CLAIMS

SUB E1 C2

1. (amended) An integrated circuit substrate comprising:

a first surface for receiving a series of aligned layers during the creation of the integrated circuit, and

a second surface disposed substantially opposite the first surface, the second surface having at least one alignment mark formed thereon prior to the first surface receiving any of the series of aligned layers during the creation of the integrated circuit, the at least one alignment mark adapted for aligning the series of aligned layers one to another during the creation of the integrated circuit.

REMARKS

Claims 1-6, 8, and 15-17 are in the case, and claims 15-17 have been withdrawn from consideration. Claims 1-3, 5-6, and 8 are rejected under 35 USC § 102 over Glenn et al. Claim 4 is rejected under 35 USC § 103 over Glenn et al. in view of Fujimura. The abstract is objected to, and is amended herein. Claim 1 is hereby amended. No new matter has been introduced by the amendments, which are supported by the disclosure of the original claims and the specification. Reconsideration and allowance of the claims are requested.

SPECIFICATION OBJECTIONS

The abstract is objected to, presumably because it is 101 words long. The specification is hereby amended as given above to remove one word. Reconsideration and withdrawal of the objection are respectfully requested.

CLAIM REJECTIONS UNDER §102

Claims 1-3, 5-6, and 8 are rejected under 35 U.S.C. 102 as being unpatentable over Glenn et al. Independent claim 1 as amended claims, *inter alia*, an integrated circuit substrate having a first surface for receiving a series of aligned layers during the creation of the integrated circuit, and a second surface disposed substantially opposite the first surface, the second surface having at least one alignment mark formed thereon prior to the first surface receiving any of the series of aligned layers

during the creation of the integrated circuit, the at least one alignment mark adapted for aligning the series of aligned layers one to another during the creation of the integrated circuit.

Thus, claim 1 as amended claims structure that distinguishes over the cited references, as described in more detail below. Claim 1 claims a substrate that has a backside alignment mark prior to the commencement of any fabrication processes for the integrated circuit.

Glenn et al. do not describe such a substrate. Glenn et al. describe a substrate that already has all of the aligned layers formed on it, because front side processing of the integrated circuit is completed, and the substrate is being diced into individual integrated circuits. Thus, the substrate of Glenn et al. does not have at least one alignment mark for aligning the series of aligned layers one to another, as claimed in claim 1. Glenn et al. describe a substrate that has no markings on the back side during the formation of the layers, and then receives a mark just prior to dicing, after the aligned layers have been formed and scribe lines have been defined on the front side of the substrate. Glenn et al. repeatedly describe forming the back side marks with reference to the features already formed on the front of the substrate. Therefore, Glenn et al. do not describe a substrate having markings that are used to align the layers of an integrated circuit during processing, as claimed in claim 1.

Thus, claim 1 patentably defines over Glenn et al. Reconsideration and allowance of claim 1 are respectfully requested. Dependent claims 2-3, 5-6, and 8 depend from independent claim 1, and contain additional important aspects of the invention. Therefore, dependent claims 2-3, 5-6, and 8 patentably define over Glenn et al. Reconsideration and allowance of dependent claims 2-3, 5-6, and 8 are respectfully requested.

CLAIM REJECTIONS UNDER §103

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al. in view of Fujimura. Dependent claim 4 depends from independent claim 1, and claims, *inter alia*, an integrated circuit substrate having a first surface for receiving a series of aligned layers during the creation of the integrated circuit, and a second surface disposed substantially opposite the first surface, the second surface having at least one alignment mark formed thereon prior to the first surface receiving any of the

series of aligned layers during the creation of the integrated circuit, the at least one alignment mark adapted for aligning the series of aligned layers one to another during the creation of the integrated circuit.

The deficiencies of Glenn et al. in regard to the limitations of independent claim 1 are described at length above. Fujimura does not compensate for the deficiencies of Glenn et al., in that Fujimura does not describe printing an alignment mark on the back side of the substrate prior to creating any layers of a integrated circuit on the front side of the substrate. Therefore, the combination of Glenn et al. and Fujimura does not described the substrate as claimed in claimed 4.

Thus, claim 4 patentably defines over Glenn et al in view of Fujimura. Reconsideration and allowance of claim 4 are respectfully requested.

CONCLUSION

Applicants assert that the claims of the present application patentably define over the prior art made of record and not relied upon for the same reasons as given above. A marked copy of the amendments is provided herewith. Applicants respectfully submit that a full and complete response to the office action is provided herein, and that the application is now in fully in condition for allowance. Action in accordance therewith is respectfully requested.

In the event this response is not timely filed, applicants hereby petition for the appropriate extension of time and request that the fee for the extension be charged to deposit account 12-2355. Should the examiner require further clarification of the invention, it is requested that he contact the undersigned before issuing the next office action.

Sincerely,

LUEDEKA, NEELY & GRAHAM, P.C.

By: _____

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2003.01.27

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I hereby certify that this correspondence is being transmitted by facsimile to the Patent and Trademark Office in accordance with § 1.6(d) on the date below.

2003.01.27
Date

Rick Barnes, 39,596

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MARKED COPY OF AMENDMENTS

IN THE SPECIFICATION

Please replace the abstract with the following text:

An integrated circuit substrate having a first surface for receiving a series of aligned layers during the creation of the integrated circuit, and a second surface disposed substantially opposite the first surface, where the second surface has at least one alignment mark for aligning the series of aligned layers one to another during ~~the~~ creation of the integrated circuit. An apparatus for aligning a mask having an image and at least one complimentary alignment mark to a substrate having a first surface and a substantially opposing second surface, where the substrate has at least one alignment mark on the second surface.

IN THE SPECIFICATION

1. (amended) An integrated circuit substrate comprising:

a first surface for receiving a series of aligned layers during the creation of the integrated circuit, and

a second surface disposed substantially opposite the first surface, the second surface having at least one alignment mark <u>formed thereon prior to the first surface receiving any of the series of aligned layers during the creation of the integrated circuit, the at least one alignment mark adapted</u> for aligning the series of aligned layers one to another during the creation of the integrated circuit.